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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,563	02/26/2002	Sergey Lopatin	P1410	7966

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/084,563	LOPATIN ET AL.
	Examiner	Art Unit
	Hsien-Ming Lee	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 08 May 2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Remarks

1. Applicants' cancellation to claims 5 and 15 is acknowledged.

2. Claims 1-4, 6-14 and 16-20 are pending in the application.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "a reduced-oxygen Cu-Zn alloy fill having a uniform zinc distribution" renders indefinite because of the ambiguity of " uniform zinc distribution." Does it refer to having a uniform distribution along the thickness direction or something else ? A clarification regarding this limitation is required. (Note) Due to the aforementioned ambiguity, the limitation is treated in this Office action based upon the best understanding of the Examiner.

Grounds of Rejections

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6, 10-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamoorthy et al. (US 6,486,533) in view of Miyafuji et al. (US 6,313,064).

In re claim 1, Krishnamoorthy et al. teach the claimed method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of;

- providing a semiconductor substrate having a Cu surface 35 (i.e. a bonding layer; col.4, lines 60-64) formed in a via (Fig.1);
- providing a chemical solution (i.e. an electroplating solution);
- electroplating the Cu surface 35 in the chemical solution (i.e. an electroplating solution, col.5, lines 53-55, col. 6, lines 62-67,col.7, lines 1-42), thereby forming a Cu-Zn alloy 40 fill in the via and on the Cu surface 35 (Fig.1);
- rinsing the Cu-Zn alloy fill 40 in a solvent stored in a rinsing chamber (col.9, lines 33-37);
- drying the Cu-Zn alloy fill 40 under a gaseous flow (col.9, lines 33-44);
- annealing the Cu-Zn alloy fill 40 formed in the via and on the Cu surface 35 (col.5, line 61 through col.6, line 6), thereby forming a post-annealed Cu-Zn alloy fill having a uniform zinc distribution;
- planarizing the post-annealed Cu-Zn alloy fill and the Cu surface 35, thereby completing formation of the post-annealed Cu-Zn alloy filled dual-inlaid interconnect structure (Fig.1); and
- completing formation of the semiconductor device.

Krishnamoorthy et al. is silent as to the post-annealed Cu-Zn alloy being the claimed reduced-oxygen Cu-Zn alloy.

However, one of the ordinary skill in the art would have recognized that the post-annealed Cu-Zn alloy is nothing but the reduced-oxygen Cu-Zn alloy, in light of the teachings of Miyafuji et al.. In particular, Miyafuji et al., in an analogous art of Cu-Zn alloy formation, suggest that by subjecting the as-electroplated Cu-Zn alloy to a heat treatment (i.e. the annealing) at a proper temperature the Zn in the Cu-Zn alloy would oxidize as ZnO due to the fact that Zn has far more intense affinity with oxygen than Cu. In other words, by subjecting to the heat treatment (i.e. the annealing) oxygen concentration in the Cu-Zn alloy would reduce, i.e. producing the reduced-oxygen Cu-Zn alloy.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made to, appreciate that the post-annealed Cu-Zn alloy of Krishnamoorthy et al. is the reduced-oxygen Cu-Zn alloy, since it is the inherent consequence of the annealing, as evidenced by Miyafuji et al.

In re claims 2-4, 12, 13 and 14, Krishnamoorthy et al. teach that the chemical solution (i.e. the electroplating solution) is nontoxic and aqueous, and wherein the chemical solution comprises: at least one zinc (Zn) ion source for providing a plurality of Zn ions such as $ZnSO_4$; at least one copper (Cu) ion source for providing a plurality of Cu ions such as copper sulfate ($CuSO_4$); at least one complexing agent for complexing the plurality of Cu ions such as EDTA; at least one pH adjuster such as ammonium hydroxide; at least one wetting agent for stabilizing the chemical solution such as organic additives, all being dissolved in a volume of delonized (DI) water. (col. 6, line 27 through col.7, line 29; col.8, lines 56-58).

In re claims 6 and 16, Krishnamoorthy et al. further teach that said electroplating step comprises using an electroplating apparatus (i.e. electroplating reactor, col.9, lines 12-14), and wherein said electroplating apparatus comprises: (a) a cathode-wafer 30; (b) an anode; (c) an electroplating vessel; and (d) a voltage source; and the cathode-wafer 30 comprises the Cu surface, and the anode comprises at least one material selected from copper (col.7, lines 53-53-58).

In re claim 10, Krishnamoorthy et al also teach that the annealing steps are performed in a temperature range of approximately 150 °C to approximately 450 °C (i.e. 250 ~350 °C; col.6, lines 7-26), and the annealing steps are performed for a duration range of approximately 0.5 minutes to approximately 60 minutes (i.e. 30 minutes)(col.6, lines 4-6).

In re claim 11, Krishnamoorthy et al. in view of Miyafuji et al. also teach the claimed semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, fabricated by the method as stated above.

7. Claims 1, 2, 4, 6, 7, 11, 12, 14, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 2002/0008034 A1) in view of Miyafuji et al. (US 6,313,064).

In re claim 1, Chen et al. teach the claimed method of fabricating a semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, comprising the steps of;

- providing a semiconductor substrate having a Cu surface 15 (i.e. a copper seed layer) formed in a via 5 (Fig.2B);

- providing a chemical solution (i.e. an electroplating solution);
- electroplating the Cu surface 15 in the chemical solution, thereby forming a Cu-Zn alloy 18 fill in the via 5 and on the Cu surface 15 (Fig. 2C and paragraph [0067]);
- rinsing the Cu-Zn alloy fill in a solvent (paragraphs [0082] and [0179]);
- drying the Cu-Zn alloy fill under a gaseous flow (paragraphs [0082] and [0179]);
- annealing (i.e. a thermal processing step) the as-electroplated Cu-Zn alloy fill 18 formed in the via 5 and on the Cu surface 15 (paragraphs [0069] and [0094], thereby forming a post-annealed Cu-Zn alloy fill having a uniform zinc distribution;
- planarizing the post-annealed Cu-Zn alloy fill and the Cu surface 15, thereby completing formation of the post-annealed Cu-Zn alloy filled dual-inlaid interconnect structure (Figs. 2D-2E); and
- completing formation of the semiconductor device.

Chen et al. is silent as to the post-annealed Cu-Zn alloy being the reduced-oxygen Cu-Zn alloy.

However, one of the ordinary skill in the art would have recognized that the post-annealed Cu-Zn alloy is nothing but the reduced-oxygen Cu-Zn alloy, in light of the teachings of Miyafuji et al.. In particular, Miyafuji et al. in an analogous art of Cu-Zn alloy formation suggest that by subjecting the Cu-Zn alloy to a heat treatment (i.e. the annealing) at a proper temperature the Zn in the Cu-Zn alloy would oxidize as ZnO due to the fact that Zn has far more intense affinity with oxygen than Cu. In other words, by subjecting to the heat treatment (i.e. the annealing) oxygen concentration in the Cu-Zn alloy would <u>reduce</u>, i.e. producing the reduced-oxygen Cu-Zn alloy.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to appreciate that the post-annealed Cu-Zn alloy of Chen et al. is the claimed reduced-oxygen Cu-Zn alloy since it is an inherent consequence of the annealing, as evidenced by Miyafuji et al.

In re claims 2 and 12, Chen et al. teach that the chemical solution (i.e. the electroplating solution; paragraphs [0071]-[0095]) is nontoxic and aqueous (i.e. alkaline bath), and wherein the chemical solution comprises: at least one zinc (Zn) ion source for providing a plurality of Zn ions; at least one copper (Cu) ion source for providing a plurality of Cu ions such as copper sulfate (paragraph [0073]); at least one complexing agent for complexing the plurality of Cu ions such as EDTA (paragraph [0078]); at least one pH adjuster such as ammonium hydroxide (paragraph [0079]); at least one wetting agent for stabilizing the chemical solution such as organic additives (paragraph [0095]), all being dissolved in a volume of delonized (DI) water.

In re claims 4 and 14, Chen et al. teach that at least one copper (Cu) ion source comprising copper sulfate ($CuSO_4$). (paragraph [0073])

In re claims 6 and 16, Chen et al. teach that said electroplating step comprises using an electroplating apparatus 25 as shown in Fig.3, and wherein said electroplating apparatus 25 comprises: (a) a cathode-wafer 30; (b) an anode 50; (c) an electroplating vessel; and (d) a voltage source 45; and the cathode-wafer 30 comprises the Cu surface, and the anode 50 comprises at least one material selected from a group consisting essentially of copper (Cu) and copper-zinc alloy (Cu-Zn, i.e., brass).

In re claim 11, Chen et al. in view of Miyafuji et al. also teach the claimed semiconductor device, having a reduced-oxygen copper-zinc (Cu-Zn) alloy filled dual-inlaid interconnect

structure formed on a copper (Cu) surface formed by electroplating the Cu surface in a chemical solution, fabricated by the method as stated above.

In re claims 7 and 17, Chen et al. also teach that said semiconductor substrate further comprises a barrier layer 10 (Fig.2A) formed in the via 5 under said Cu surface 15, and wherein the barrier layer comprises tantalum nitride (TaN). (paragraph [0060]).

8. Claims 8, 9, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US '034) in view of Miyafuji et al. (US '064) as applied to claims 1, 2, 4, 6, 7, 11, 12, 14, 16 and 17 above, and further in view of Dubin et al. (US 2002/0084529).

In re claims 8 and 18, Chen et al. in view of Miyafuji et al. substantially teach the claimed method and the device, as stated above, but fail to teach comprising an underlayer formed on the barrier layer, wherein said underlayer comprises at least one material selected from a group consisting essentially of tin (Sn) and palladium (Pd), and wherein said Cu surface is formed over said barrier layer and on said underlayer.

However, Dubin et al., in an analogous art (Fig.6), teach steps of: (1) forming a barrier layer 240 in a via; (2) forming an underlying layer 280A (i.e. a shut material layer) comprising tin on the barrier layer 240 (paragraphs [0039] and [0031]); (3) forming a Cu surface 290 (i.e. copper seed layer) over the barrier layer 240 and on the underlying layer 280A; and (4) forming an electroplated Cu-Zn alloy 260 on the Cu surface 290.

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to comprise the underlying layer formed on the barrier layer as taught by Dubin et al. and then to proceed the subsequent formation of the Cu-Zn alloy in the via and on the Cu surface as taught by Chen et al., since by comprising the underlying layer between the

barrier layer and the Cu surface it would improve electromigration performance of the semiconductor device. (paragraph [0044], Dubin et al.)

In re claims 9 and 19, Chen et al. teach that the Cu surface 15 comprises a thickness range of approximately 50~500 Å (paragraph [0062]), which is within the claimed range. As far as the selections of the thickness of the underlying layer, the barrier layer and the Cu-Zn alloy are concerned, it is obvious to one of the ordinary skill in the art because it is a matter of determining optimum process condition by routine experimentation. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the thickness of the barrier layer can be optimized to thin enough to inhibit material diffusion between adjacent layers (paragraph [0023], Dubin et al.). The thickness of the underlying layer can be selected at a proper range to enough enhance the electromigration performance of the semiconductor device but not to compromise the step coverage in the via (paragraph [0044], Dubin et al.). In addition, the thickness of the Cu-Zn alloy can be optimized to repair or enhance the Cu surface but not too thick to interfere the subsequent metal filling. (paragraph [0065], Chen et al.) In this case, applicants are required to demonstrate the criticality, generally by showing that the claimed thickness would achieve <u>unexpected</u> results relative to the prior art range. See M.P.E.P 2144.05 III

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claim 20 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,515,368. Although the conflicting claims are not identical, they are not patentably distinct from each other because the Patent and the application are claiming common subject matter, regardless the obvious variation, wherein the obvious variation refers to the Patent reciting " Cu-Zn alloy thin film", whereas the application reciting " Cu-Zn alloy fill."

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to recognize that the instant invention is not patentably distinguish over the prior art.

Response to Arguments

11. Applicant's arguments filed 5/8/03 have been fully considered but they are not persuasive.

Applicants argue that Krishnamoorthy et al do not teach or suggest the claimed method mainly because Krishnamoorthy et al require a dielectric layer 25 and a bonding layer 35, whereas the present invention does not require either a bonding layer or a dielectric layer. Applicants further argue that Krishnamoorthy et al do not teach the limitation "directly

depositing of electrically conductive interim Cu-Zn alloy on a Cu surface." (last paragraph of page 11 through first paragraph of page 12).

In response to the arguments, it is submitted that the present invention merely claims "providing a semiconductor substrate **having a Cu surface** formed in a via" (claim 1, line 5). (Emphasis added) Since Krishnamoorthy et al teach providing a semiconductor substrate ***having a Cu surface 35*** (col.4, lines 60-64) formed in a via, regardless of the terminology difference, it is obvious that Krishnamoorthy et al do teach the limitation "a semiconductor substrate having a Cu surface."

In response to the argument that Krishnamoorthy et al do not teach the step of "**directly depositing** of electrically conductive interim Cu-Zn alloy on a Cu surface, it is submitted that the limitation " directly depositing" is ***not in the claim***. Claim 1, lines 7-8, merely recites "**electroplating** the Cu surface **in the chemical solution**, thereby forming a Cu-Zn alloy fill in the via and on the Cu surface." (Emphasis added).

Since Krishnamoorthy et al disclose the claimed step of "electroplating the Cu surface in the chemical solution, thereby forming a Cu-Zn alloy fill in the via and on the Cu surface, as stated in the rejection, the teachings of Krishnamoorthy et al read on the limitation.

As far as the claimed limitation " reduced-oxygen Cu-Zn alloy" (claim 1, lines 11-12) is concerned, applicants argue that Miyafuji's teachings do not remedy the deficiency of Krishnamoorthy et al because Miyafuji teach away from the problems sought to be solved by the present invention (second paragraph, page 12).

In response to the argument, Krishnamoorthy et al teach "annealing the Cu-Zn alloy fill 40 formed in the via and on the Cu surface 35 (col.5, line 61 through col.6, line 6), thereby

forming a post-annealed Cu-Zn alloy fill." Since Krishnamoorthy et al teach the same claimed processing step (i.e. the annealing) for treating the same material (i.e. as-electroplated Cu-Zn alloy), it would have been obvious to one of the ordinary skilled in the art to recognize that it would produce the same product, i.e. "reduced-oxygen Cu-Zn alloy ." In order to support this position, Miyafuji reference is used. Miyafuji clearly suggest why the post-annealed Cu-Zn alloy being the "reduced-oxygen Cu-Zn alloy" is that ***Zn has far more intense affinity with oxygen than Cu*** (col.4, lines 57-66). By subjecting the as-electroplated Cu-Zn alloy to the annealing step, zinc in the Cu-Zn alloy would attract oxygen because of its higher affinity with oxygen than with copper, causing removing oxygen from the Cu-Zn alloy and thus forming the "reduced-oxygen Cu-Zn alloy."

Applicants further argue that cited references do not teach the production of a reduced-oxygen Cu-Zn alloy fill having a uniform zinc distribution. In response to the argument, it is submitted that ***similar process*** can reasonably be expected to yield product which inherently have the ***same properties***. *In re* Spada 15 USPQ2d 1655 (CAFC 1990); *In re* DeBlauwe 222 USPQ 191; *In re* Wiegand 86 USPQ 155 (CCPA 1950). Since Krishnamoorthy et al utilize the same process (i.e. annealing) to treat the same material (i.e. as-electroplated Cu-Zn alloy), it can reasonably be expected to form the claimed product "reduced-oxygen Cu-Zn alloy fill ***having a uniform zinc distribution***." (Emphasis added) In addition, there appears ***no descriptive support*** in the original filled specification as to ***how to arrive*** the product having the ***uniform zinc distribution.*** The instant invention, thus, ***cannot patentably distinguish*** over the prior art.

Therefore, the rejection to claims 1-4, 6, 10-14 and 16 under 103(a) is deemed proper.

Applicants further argue that Chen et al. do not teach the claimed invention because Chen et al. do not disclose "a cathode-wafer surface which receives an equal potential voltage distribution across the entire wafer while being submerged in the electroplating bath." (second paragraph, page 15)

In response to the argument, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, the 103(a) rejection to claims 1, 2, 4, 6, 7, 11, 12, 14, 16 and 17 over Chen et al. in view of Miyafuji et al. is deemed proper.

In response to applicants' arguments against the references individually, i.e. Dubin et al. reference, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Lastly, applicants argue that US 6,515,368 neither teach nor suggest the present invention because of the recitation " ***a Cu-Zn alloy layer as a thin film layer 30*** " in claim 1 of US '368 versus the limitation "**a Cu-Zn alloy fill 30 is the dual-inlaid interconnect structure"** in claim 20 of the instant invention.

In response to the argument, it is submitted that both US '368 and the instant invention claim a common subject matter, regardless obvious variation. The only difference between US '368 and the instant invention was that US '368 recites " reduced-oxygen copper-zinc alloy (Cu-Zn) thin film ", whereas the instant invention recites "reduced-oxygen Cu-Zn alloy." Furthermore, US '368 also recites "dual-laid interconnect structure." (at line 8 of claim 1)

Therefore, it would have been obvious to one of the ordinary skill in the art to recognize that although the conflicting claims are not identical, they are not patentably distinct from each other for the reasons above. The double patenting rejection to claim 20, is thus deemed proper.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

July 17, 2003

W. David Coleman
Primary Examiner